Remarks/Arguments:

Applicants' disclosure is directed to a gate driver for forcing a power transistor having a gate electrode to either conduct or shut off. The gate driver includes a first current source and a second current source. The first current source outputs a first current that lowers the electric potential of the gate electrode and causes the power transistor to begin conducting The second current source outputs a second current that raises the electric potential of the gate electrode and causes the power transistor to shut off. Current-source control information determines the value of the first current and the second current, respectively. Accordingly, the first current controls the time it takes to fully shut off the power transistor and the second current controls the time it takes to cause the power transistor to begin fully conducting.

Claims 1 and 3 stand rejected under 35 U.S.C. § 102(b) as anticipated by Hsiao et al. (U.S. Patent No. 6,437,611). Claim 5 stands rejected under 35 U.S.C. § 103(a) as obvious over Hsiao and Kogushi (U.S. Patent No. 6,236,239). It is respectfully submitted, however, that the claims are patentable over the art of record for the reasons set forth below.

Hsiao discloses a circuit for pulling up or pulling down a voltage level of an output node of the circuit. Transistors 220 and 225 are connected to the gate of transistor 240 so as to instantly turn output transistor 240 on or off depending on a level of an input received at the gates of transistors 220 and 225. Similarly, transistors 230 and 235 are connected to the gate of transistor 245 so as to instantly turn transistor 245 on or off depending on a level of an input received at the gates of transistors 230 and 235.

Kogushi is directed to an output-buffer circuit. The circuit includes two pairs of transistors 4/5 and 6/7, a bias circuit 21 and two output transistors 10 and 11. The output of the bias circuit controls the value of the current output from each pair of transistors, respectively. The transistors pairs are operable to apply different currents to the output transistors to control the turn on time of the output transistors. However, the circuit also provides switch off transistors 12 and 13 for instantly

changing the state of its corresponding output transistor from a conductive state to a shut off state.

Applicants' invention, as recited by claim 1, includes a feature which is neither disclosed nor suggested by the art of record, namely;

> ... a first current source for outputting a first current value to raise an electric potential of the gate electrode in a time corresponding to a charging time of said input capacitance, when changing the power transistor from the shut-off state to the conductive state ...
>
> ... a second current source for outputting a second current value to decrease an electric potential of the gate electrode in a time corresponding to said input capacitance, when changing the power transistor from the conductive state to the shut-off state ... .

In the exemplary embodiment described in Applicants' disclosure, this means that a level of current output by the first current source controls the turn on time of the output transistor and a level of current output by the second current source controls the turn off time of the output transistor. Thus, turn on and turn off times of the output transistor are both controllable. This feature is found in the originally filed application at page 11, line 24-27; page 12, lines 3-4; page 12, lines 10-12; page 12, lines 19-26; and page 13, line 7. No new matter has been added.

As shown in Fig. 2(a), Hsiao discloses a circuit for pulling up or pulling down a voltage level of an output node of the circuit. The circuit relevantly includes transistors 225 and 230 for turning on output transistors 240 and 245, respectively, and includes transistors 220 and 235 for shutting off output transistors 240 and 245, respectively. This construction allows only for instant turn on and turn off of the output transistors.

As shown in Fig. 1, for example, Kogushi discloses an output buffer circuit. The circuit includes two pairs of transistors 4/5 and 6/7. The level of the current output by 4/5 and 6/7 is based on the values of VP and VN that bias circuit 21 applies respectively to 4/5 and 6/7. The level of the current output by 4/5 and 6/7 determines a turn on time of output transistors 10 and 11. The circuit further includes shut off transistors 12 and 13 for instantly shutting off output transistors 10 and 11,

respectively. Accordingly, this construction does not provide for control of the shut off time of the output transistors.

This is different because Applicants' circuit construction includes two variable current sources to control the turn on time and turn off time of the output transistor. As shown in Fig. 1, current assignor 4 assigns respective current values to current sources 31 and 32. The current values output by current sources 31 and 32 control the turn on time and turn off time of the output transistor. Hsiao discloses two pairs of transistors for turning on and turning off output transistors. However, because the pairs are simply made up of transistors, and not variable current sources as Applicants disclose, the transistors are not operable to control the turn on and turn off time of the output transistors. Further, Kogushi discloses two transistor pairs. The transistor pairs are arranged in the circuit so as to control only the turn on time of the output transistor. Because Kogushi also includes shut off transistors, the shut off transistors instantly shut off the output transistor. Accordingly, Kogushi also does not disclose use of two variable current sources configured to control the turn on and turn off time of an output transistor.

It is because Applicants include the feature of

> ... a first current source for outputting a first current value to raise an electric potential of the gate electrode in a time corresponding to a charging time of said input capacitance, when changing the power transistor from the shut-off state to the conductive state ...
>
> ... a second current source for outputting a second current value to decrease an electric potential of the gate electrode in a time corresponding to said input capacitance, when changing the power transistor from the conductive state to the shut-off state ... .

that the following advantages are achieved. Namely, the time it takes an output transistor to fully turn on or fully turn off can be controlled. This allows for restriction of noise, prevention of operating error and prevention of breaking of the power transistor.

Accordingly, for the reasons set forth above, claim 1 is patentable over the art.

Claims 3 and 5 include all the features of claim 1 from which they depend. Thus, claims 3 and 5 are also patentable over the art for the reasons set forth above.

In view of the amendments and arguments set forth above, the above-identified application is in condition for allowance, which action is respectfully requested.

Respectfully submitted,

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